AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 2, line 13, with the following rewritten paragraph:

The digital TV receiver having the above structure may have an extra tuner for an analog signal. The American Television System Committee (ATSC) standard, a type of digital broadcasting scheme, adopts various frame rates for a digital signal, including 60 Hz, 59.94 Hz, 30 Hz, ~~29.94 Hz,~~ 29.97 Hz, 24 Hz and 23.97 Hz. Thus, it is necessary to convert the clock frequency of the digital TV receiver selectively according to the frame rate of the digital signal, thereby preventing omission or redundancy in signal processing.

Please replace the paragraph beginning at page 2, line 31, and continuing on page 3, with the following paragraph:

Preferably, the first phase locked loop generates a clock frequency of 74.25 MHz and the second phase locked loop generates a clock frequency of ~~74.175 MHz.~~ 74.176 MHz. Additionally, it is preferred that when the frame rate of the input digital signal is 60 Hz, 30 Hz or 24 Hz, the controller controls the switching portion to select the clock frequency from the first phase locked loop, and when the frame rate of the input digital signal is 59.94 Hz, 29.97 Hz or 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop.

Please replace the paragraph beginning at page 4, line 6, with the following paragraph:

FIG. 3 is a detailed circuit diagram of the PLL 208 of FIG. 2. As shown in FIG. 3, the PLL 208 includes a first PLL 208a, a second PLL 208b and a switching portion 208c. The first PLL 208a includes a phase comparator 302, a low pass filter 304, a voltage controlled oscillator (VCO) 306 and a frequency divider of 1/N 308. The second PLL 208b includes a phase comparator 402, a low pass filter 404, a VCO 406 and a frequency divider of 1/N 408. In this embodiment, the first PLL 208a generates a clock frequency of 74.25 MHz and the second PLL 208b generates a clock

frequency of ~~74.175 MHz~~. 74.176. The switching portion 208c selectively outputs the clock frequency of 74.25 MHz or ~~74.175 MHz~~ 74.176 MHz according to a selection signal from the controller 212.

Please replace the paragraph beginning at, page 4, line 16, with the following paragraph:

The various frame rates of a digital signal according to the ATSC standard, including 60 Hz, 59.94 Hz, 30 Hz, ~~29.94 Hz,~~ 29.97 Hz, 24 Hz and 23.97 Hz, are classified into one of two groups: a first group including 60 Hz, 30 Hz and 24 Hz, and a second group inducing 59.94 Hz, ~~29.94 Hz~~ 29.97 Hz and 23.97 Hz.

Please replace the paragraph beginning at page 4, line 26, with the following paragraph:

Also, when an NTSC signal with a frame rate of 59.94 Hz, which is included in the second group, is input via the ADC 204,, the controller 212 controls the switching portion 208c to select the clock frequency of ~~74.175 MHz~~ 74.176 MHz from the second PLL 208b. In this case, the video decoder 202 does not operate. Thus, the controller 212 controls the buffer 210 to block the provision of the clock frequency CLOCK to the video decoder 202, such that the clock frequency CLOCK is provided to only the format converter 206 and the OSGM 214.